Electronics and DAQ Status Report

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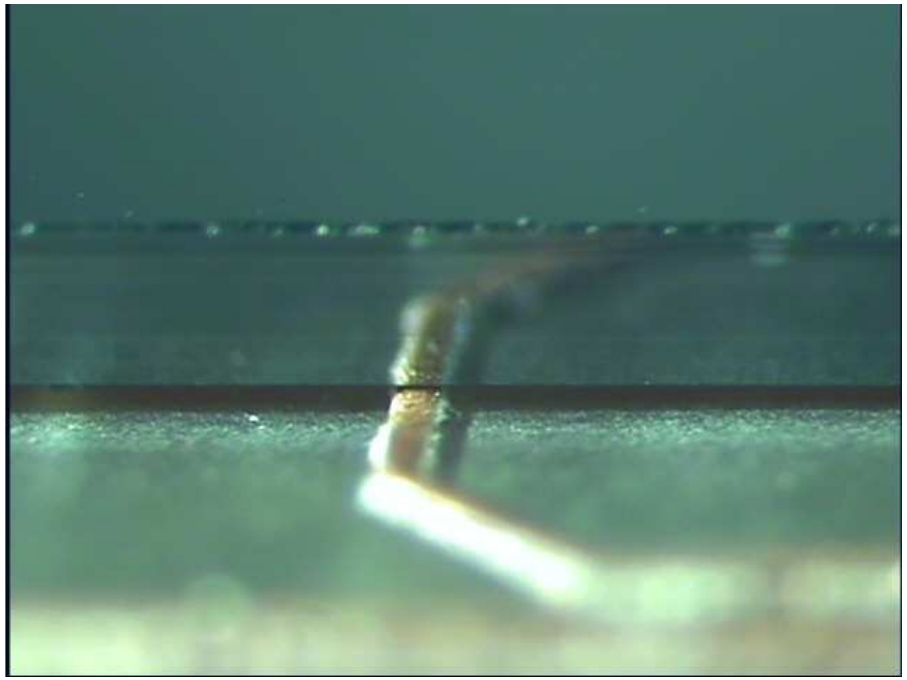
Electronics and DAQ

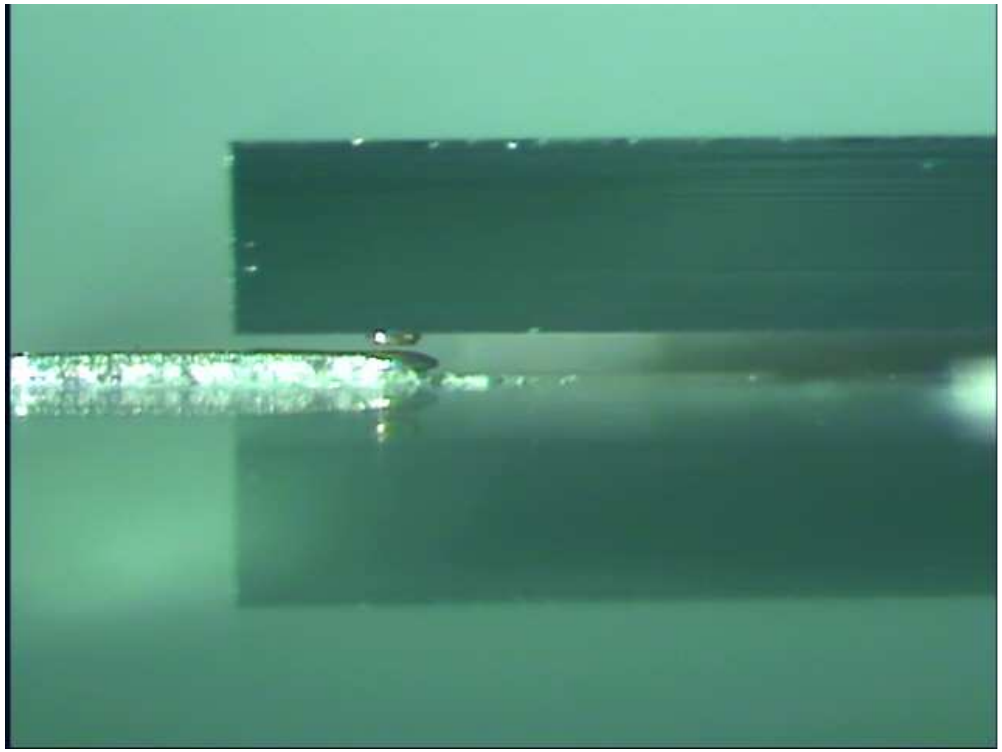
- DAQ/Elec Workshop (May 9-10)
  - Defined interface and data flow between FEB, DCM, and DAQ
  - Get pulse height and time bin (62.5ns bins)
  - Defined data rates, startup procedures
  - Segmentation issues, run control
  - Began slow control definition
  - Data rates expected to be lower by about 4x
    - (more realistic simulation of muons)

APD Status

- Version 1 with Hamamatsu
- What we learned
  - Full carrier board flatness to 1mil
    - Add Requirement for manufacturing
  - No exposed metal protruding from under APD
    - At least 2 solutions
      - Double application of epoxy at Hamamatsu
      - 4 layer board with vias to submerge traces
    - Performing both for prototypes, boards should be out for production this week
  - Why Hamamatsu gave us 20k$ off for doing this ourselves

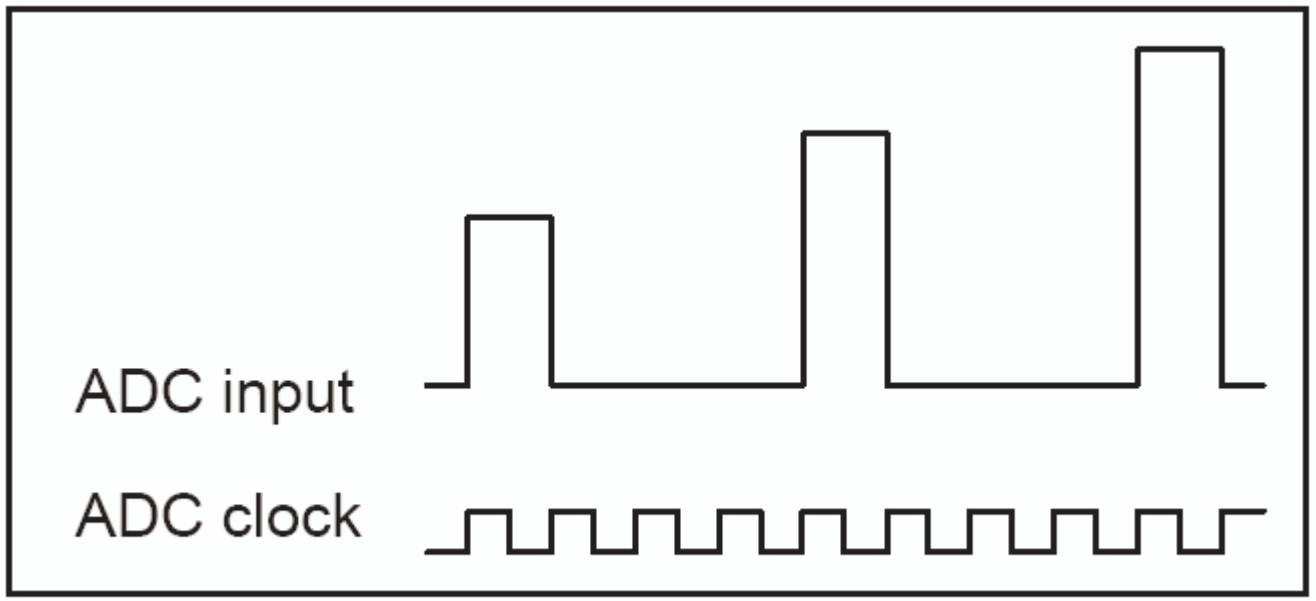
Hamamatsu Pictures





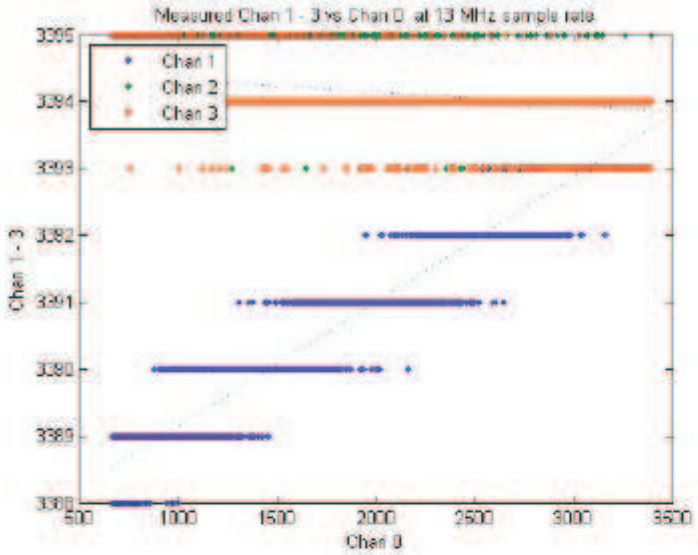
ADC Testing

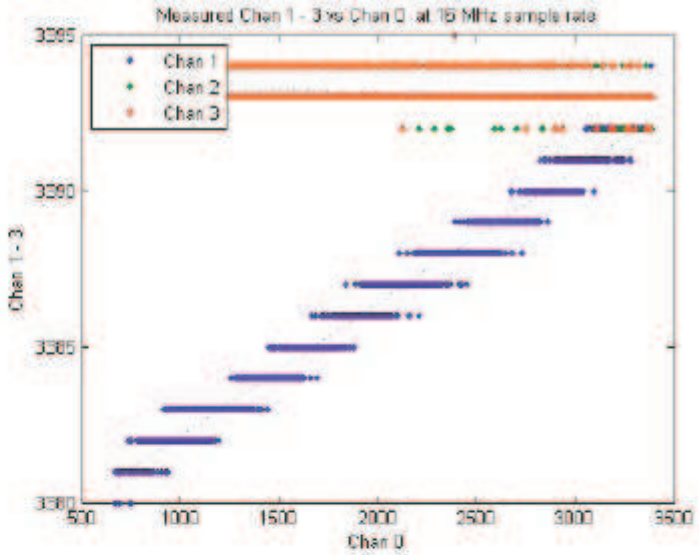
- Prototype tested by Harvard group, John, Josh, and Nathan.

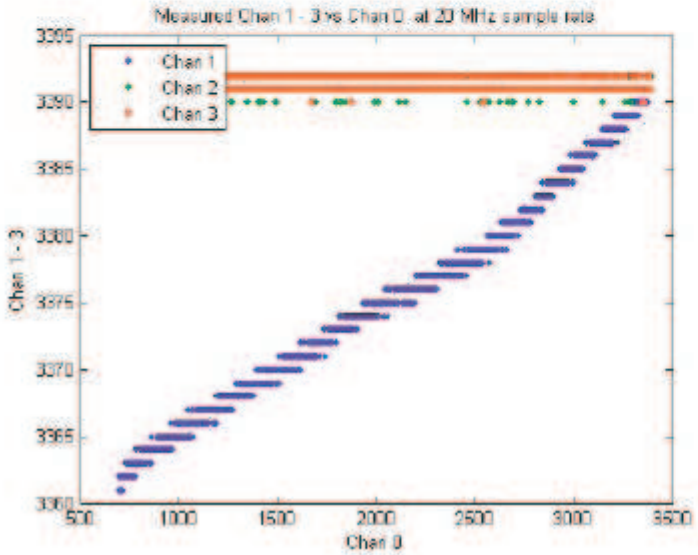


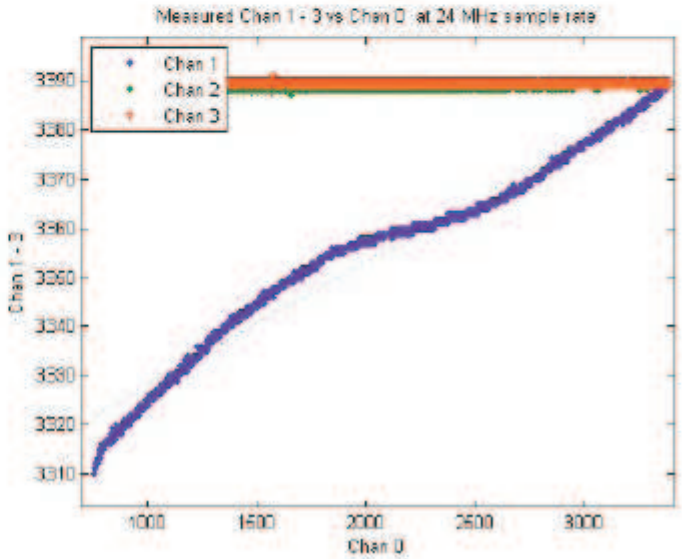
Crosstalk Measurement

- Varied Sample Frequency 13 to 24MHz
- Proposed 16MHz



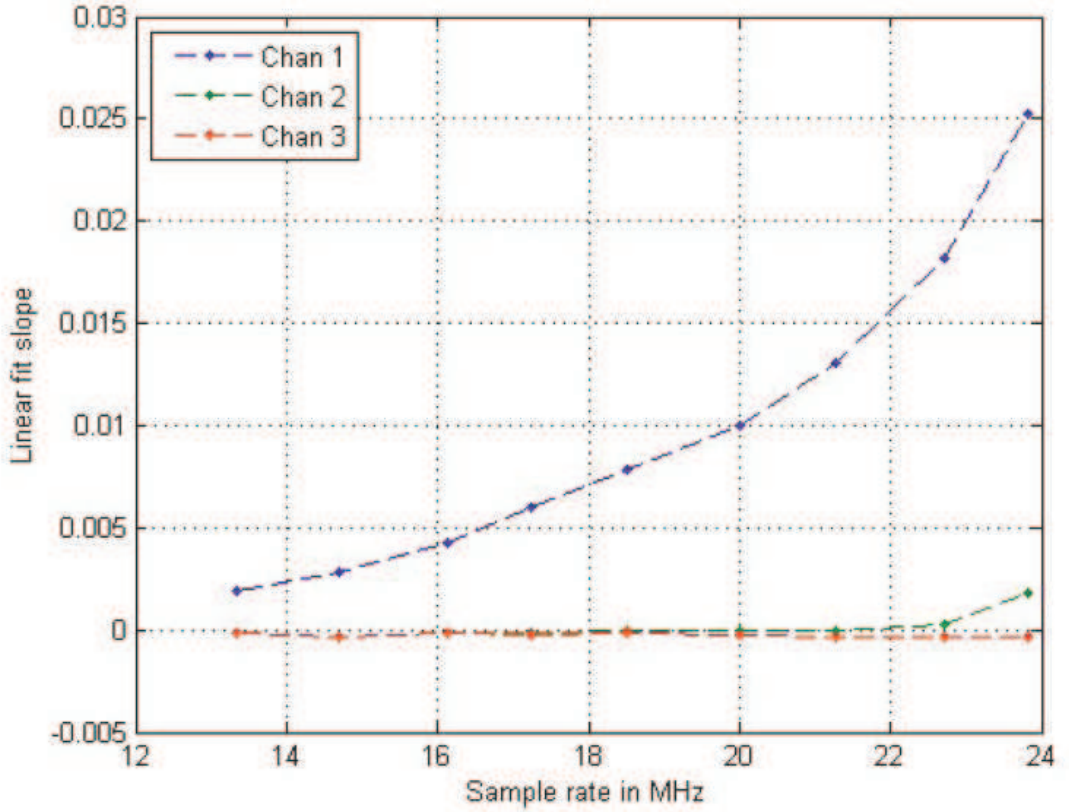






Results

- Crosstalk Maximum 0.4% ~2σ
- Threshold=~6σ



ADC conclusions

- Crosstalk 0.4%
  - invisible
- ADC pedestal <0.5 LSB
  - Negligible (expect ~8bits with APD)
- ADC linearity <0.35 LSB
  - Far better than we need
- ADC suitable for our use

FEB - Development

- Preliminary DSP tests for timing & Pulse-height extraction – Completed 2005
- Series of 4 prototype FEBs (under 1.6.2)
  - #1
    - Certification of AD41240* (4 ch, 40 Ms/s, 12-bit, custom ADC as used by CMS/HCAL – “Chipideas” Corp.) on FEB @ 16 Ms/s
    - Firmware development
    - USB interface
    - No ASIC
    - No interface to APD module or TE cooler
    - No interface to Data Concentrator
    - Currently under test
  - #2
    - Add ASIC & interface to APD module
    - Firmware development (con’t)
    - Add TE cooler controller
    - Retain USB
    - Detector “ready”

Development Plan – con’t

- #3
  - Replace USB with DAQ interface to Data Concentrator Module (DCM)
  - Firmware development (con’t)
  - Detector “ready”

- #4
  - Final production ready prototype
  - Firmware development (con’t)
  - To be produced in qty ~ 400 for Integration Prototype Near Detector (IPND)

ASIC Status

- Prototype production parts under test
- Very flexible prototype chip
  - Multiple modes
    - Continuous Muxed output (BASELINE)
      - External Quad 12bit 40MS/s ADC
    - SCA Mode
      - 64 sample capacitors per channel, depth 32us
      - Onboard 10bit Wilkinson ADC
    - Continuous on-board digitization
      - “Floating point” Wilkinson ADC
  - Multiple front-ends
    - Varied input transistor parameters to determine optimal parameters for best noise performance

Prototype Performance

- Integrator
  - Performs as expected
  - Nominal gain 10mV/fC==10mV/6250e-
  - ==1mV/625e-
- Shaper stage
  - Programmable gain (2-10X)
    - Overall Sensitivity 62.5-313e-/mV
  - Programmable rise time output (50-500ns)
  - Programmable fall time determined by external resistor

Mux Output Performance

- Differential output
- Risetime of 30-40ns to 0.1% when driving a load of ~30pF
- Maximum output crosstalk <0.5%
  - More to be done on this, may depend on how the ADC load appears to the mux
  - More testing on this to be done in coordination with Harvard characterization of ADC

Noise Performance

- Noise measured using on-board ADC
- ADC works!
- Noise Simulations expect 150e-
  - 10pF detector capacitance
  - 250ns shaping time
  - 1us dual correlated sampling with onboard ADC
- Measured noise 154e- under same conditions on bench

ASIC Conclusions

- Device works!
- Future work
  - Test different input configurations to see if even better match is possible
  - Investigating packaging possibilities
    - With 32 inputs, a 128 pin package would allow connections for all modes to be brought out
  - Once packaged, it will be used on the next FEB prototype

Conclusions

- APD
  - Expect to send next version of carrier to Hamamatsu in ~2 weeks. Once OK'd, we will machine holes and send them for APD mounting. Really need a working module by August.
- ASIC prototype works!
- FEB
  - Prototype II under design, incorporates new ASIC, ADC, USB readout, APD interface.
  - Detector ready prototype version, just has different interface.
  - Attempting to accommodate the board width in the thickness of the module.
- DAQ
  - Development continues
  - Data rates lower, ~4X,